01-25-01 09/744465 PCT

U.S. Application No. Unknown | International Application No. PCT/BE99/00090 | Attorney Docket No. **IMEC228.001APC**

Date: January 23, 2001

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 USC 371

International Application No.:	PCT/BE99/00090
International Filing Date:	July 14, 1999
Priority Date Claimed:	July 24, 1998
Title of Invention:	A SYSTEM AND A METHOD FOR PLATING OF A CONDUCTIVE PATTERN
Applicant(s) for DO/EO/US:	Filip Van Steenkiste; Kris Baert; Walter Gumbrecht; Philippe Arquint

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. (X) This is a **FIRST** submission of items concerning a filing under 35 USC 371.

2. () This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 USC 371.

3. (X) This express request to begin national examination procedures (35 USC 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 USC 371(b) and PCT Articles 22 and 39(1).

4. (X) A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. (X) A copy of the International Application as filed (35 USC 371(c)(2))

   a) () is transmitted herewith (required only if not transmitted by the International Bureau).
   b) (X) has been transmitted by the International Bureau.
   c) () is not required, as the application was filed in the United States Receiving Office (RO/US).

6. (X) A translation of the International Application into English (35 USC 371(c)(2)).

7. (X) Amendments to the claims of the International Application under PCT Article 19 (35 USC 371(c)(3))

   a) () are transmitted herewith (required only if not transmitted by the International Bureau).
   b) () have been transmitted by the International Bureau.
   c) (X) have not been made; however, the time limit for making such amendments has NOT expired.
   d) (X) have not been made and will not be made.

8. () A translation of the amendments to the claims under PCT Article 19 (35 USC 371(c)(3)).

9. () An oath or declaration of the inventor(s) (35 USC 371(c)(4)).

10. (X) A copy of the International Preliminary Examination Report with any annexes thereto, such as any amendments made under PCT Article 34.

11. () A translation of the annexes, such as any amendments made under PCT Article 34, to the International Preliminary Examination Report under PCT Article 36 (35 USC 371(c)(5)).

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Items 11. to 16. below concern other document(s) or information included:

12.	()	An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
13.	()	An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
14.	()	A FIRST preliminary amendment.
	()	A SECOND or SUBSEQUENT preliminary amendment.
15.	()	A substitute specification.
16.	()	A power of attorney and/or address letter.
17.	(X)	International Application as published.
18.	()	Small Entity Statement.
19.	(X)	PCT Form PCT/IPEA/402.
20.	(X)	PCT Form PCT/IB/308.
21.	()	PCT request form.
22.	()	Other Items or information:
23.	(X)	A return prepaid postcard.

24. (X) The following fees are submitted:

				FEES
	BASIC FEE			$1,000
CLAIMS	**NUMBER FILED**	**NUMBER EXTRA**	**RATE**	
Total Claims	14 - 20 =	0 ×	$18	$0
Independent Claims	3 - 3 =	0 ×	$80	$0
Multiple dependent claims(s) (if applicable)			$270	$0
	TOTAL OF ABOVE CALCULATIONS		$0	
Reduction by 1/2 for filing by small entity (if applicable). Verified Small Entity statement must also be filed. (NOTE 37 CFR 1.9, 1.27, 1.28)			$0	
	TOTAL NATIONAL FEE			$860
	TOTAL FEES ENCLOSED			$860

25. (X) The fee for later submission of the signed oath or declaration set forth in 37 CFR 1.492(e) will be paid upon submission of the declaration.

26. (X) A check in the amount of $860 to cover the above fees is enclosed.

27. () Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40 per property.

28. (X) The Commissioner is hereby authorized to charge only those additional fees which may be required, now or in the future, to avoid abandonment of the application, or credit any overpayment to Deposit Account No. 11-1410. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

KNOBBE, MARTENS, OLSON & BEAR, LLP
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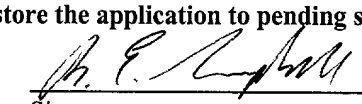
Sixteenth Floor
Newport Beach, CA 92660


Signature

Richard E. Campbell
Printed Name

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Registration Number

A SYSTEM AND A METHOD FOR PLATING OF A CONDUCTIVE PATTERN

Field of the invention

The invention relates to methods and systems for plating conductive patterns.

Technological background

In the solid state electronics industry, a plurality of components being active devices as well as passive devices are processed on a surface of a semiconductor wafer for instance to form an integrated circuit. To form these integrated circuits metallization structures are requested both as a part of the aforementioned devices and to interconnect these devices. The formation of such metallization structures includes the plating of a conductive pattern, being part of a metallization structure and being formed at a first surface of a substrate, such as a wafer. Particularly this first surface can be the front side or the back side of the wafer.

One of the issues involved is the plating of this first surface of a substrate without exposing a second surface of a wafer, opposite to the first surface, to a plating solution. Particularly, exposure, even partly, would result in unwanted wetting, plating and/or corroding of other surfaces. Furthermore to be able to deposit a material by electroplating, the plating solution must be in contact with the first surface of the substrate comprising

the conductive patterns to be plated and two electrically connectable electrodes have to be provided. Usually, the first electrode is immersed in the plating solution, while the second electrode has to be electrically connected to the conductive patterns to be plated. State-of-the-art plating techniques usually contact peripheral regions of the first surface of a substrate, comprising the conductive patterns to be plated. These peripheral contact regions are electrically connected to the second electrode as well as to the conductive patterns to be plated.

A problem is that often long metal lines are required to connect each conductive pattern to be plated with the contact in the peripheral region. Particularly, this is a problem when one wants to perform plating on wafer scale because the differences in distance between conductive patterns to be plated being located near the edges of the wafer and in the center of the wafer are huge. These differences are typically in the centimeter range. Consequently also the differences in resistance of the metal lines connecting the respective conductive patterns can be huge. This often results in a highly non-uniform plating process. All these metal connections between the conductive patterns to be plated and the peripheral regions can not be easily removed after the plating process and moreover, a lot of wafer-area is required to provide these connections thereby inhibiting dense integration. Another problem is that the contact means in the peripheral regions are exposed to the plating solution. These contact means become parasitically plated and have to be cleaned regularly. A further problem can arise if the contact means do not simultaneously can be used as sealing means, then extra sealing means are required. These sealing means should then be positioned between the contact means and the edges of the wafer in order to avoid leakage of the plating

solution to another surface of the wafer. Consequently, this leads again to a further decrease of the available area which can be plated.

Aim of the invention

The invention presents methods and systems for plating conductive patterns which at least result in a high uniformity and avoid parasitical plating effects.

Summary of the invention

In an aspect of the invention a plating system is disclosed for plating on a plurality of conductive patterns formed at a surface of a substrate. A plating solution is applied on this surface and the exposure of other surfaces of the substrate to the plating solution is inhibited. A first electrode of the system is immersed in the plating solution while the second electrode is in contact with another surface of the substrate. The conductive patterns to be plated are temporary electrically connected with the second electrode resulting in a uniform and selective deposition over the exposed surface of the substrate. Particularly, according to this aspect of the invention, a system is disclosed for plating on at least one conductive pattern, said conductive pattern being positioned at a first surface of a substrate having at least a first surface and a second surface, said system comprising:

a support with an electrically connectable electrode thereon;

a sealing element to inhibit the exposure of the second surface of the substrate to a plating solution; and

wherein said substrate is placeable on said support such that said electrode is in contact with said

second surface of said substrate and wherein a contact to said first surface of said substrate is provided, said conductive pattern being temporary electrically connected with said contact and said contact being electrically connected with said electrode.

In another aspect of the invention, a substrate is disclosed having at least a first surface and a second surface opposite to said first surface, said first surface being exposable to a plating solution, said substrate comprising

a conductive pattern being positioned at said first surface of a substrate;

a contact to the first surface of the substrate; and

said conductive pattern being temporary electrically connected by a polysilicon or an amorphous silicon conductor with said contact and said contact being electrically connected with said second surface.

In a further aspect of the invention, a method is disclosed for plating on at least one conductive pattern formed at a surface of a substrate, said substrate having at least a first surface and a second surface, said method comprising the steps of:

placing the substrate on an electrode being part of a plating holder such that said second surface of said substrate is in contact with said electrode and said conductive pattern is temporary electrically connected to said conductive pattern; and

applying a plating solution on said first surface of said substrate thereby inhibiting exposure of said second surface to said plating solution.

Brief description of the drawings

Figure 1 shows a plurality of structures to be plated. Each one of said plurality of structures (with boundary (2)) is connected to a polysilicon stripe which crosses the dicing line (1).

Figure 2 shows a metal (3) of a first die and a second die, being adjacent. The polysilicon stripe (4) extends from said metal (3) over the dicing line (1) and is further connected to the substrate contact (5) on said second die.

Figure 3 shows a system for plating, comprising of a plating holder with a backside contact. Means for sealing (6), preventing the second surface of the wafer being exposed to the plating solution are foreseen. A backside contact means is also present.

Figure 4 shows a cross-section view of the polysilicon stripes. Dicing over the polysilicon stripe, results in disconnecting the electroplated structures from the substrate contact.

Figure 5 shows a top vies of the polysilicon stripes.

Description of the invention

In an aspect of the invention a plating system is disclosed for plating on a plurality of conductive patterns formed at a surface of a substrate. A plating solution is applied on this surface and the exposure of other surfaces of the substrate to the plating solution is inhibited. A first electrode of the system is immersed in the plating solution while the second electrode is in contact with another surface of the substrate. The conductive patterns to be plated are temporary electrically connected with the second electrode resulting in a uniform and selective deposition over the exposed surface of the

substrate. Particularly, according to this aspect of the invention, a system is disclosed for plating on at least one conductive pattern, said conductive pattern being positioned at a first surface of a substrate having at least a first surface and a second surface, said system comprising:

a support with an electrically connectable electrode thereon;

a sealing element to inhibit the exposure of the second surface of the substrate to a plating solution; and

where said substrate is placeable on said support such that said electrode is in contact with said second surface of said substrate and wherein a contact to said first surface of said substrate is provided, said conductive pattern being temporary electrically connected with said contact and said contact being electrically connected with said electrode. Particularly, the electrical connection between the contact at the first surface of the substrate and the electrode at the second surface of the substrate can be a doped semi-conductive region of either an n-type conductivity or a p-type conductivity, or a metal via connection extending from the first surface to the second surface of the substrate. Furthermore, a metal contact can be provided at the second surface of the substrate.

In an embodiment of the invention a system is disclosed for plating on a plurality of conductive patterns formed at a surface of a substrate. Each conductive pattern to be plated is temporary electrically connected with a contact to the first surface of the substrate by a polysilicon conductor or an amorphous silicon conductor. Particularly, the conductive pattern is positioned on a first die and the corresponding contact is positioned on a

second die different from said first die. Preferably said second die is adjacent to said first die to keep the polysilicon or amorphous silicon conductor as short as possible to minimize the resistance of the connection. Consequently the plating can be performed in a substantially uniform manner.

In another embodiment of the invention a system is disclosed for plating on a plurality of conductive patterns formed at a surface of a substrate, where at least a part of a conductive pattern and/or a contact to a first surface of a substrate is covered with a layer to inhibit plating on said part. Particularly this layer can be a resist layer. By doing so the usually undesired plating of a contact to the first surface of the substrate can be avoided.

The substrate can be a piece of a conductive material or a doped semi-conductive material. Particularly a silicon semiconductor wafer of a n-type or p-type conductivity can be used. The plating solution can be any commercially available plating solution. Of particular interest are plating solutions containing an element selected from a group comprising Ag, Cu, Au, Pt, Ti, Ni and Co. The conductive patterns are usually metal patterns. Particularly Al-containing or Cu-containing patterns can be used.

In another aspect of the invention, a substrate is disclosed having at least a first surface and a second surface opposite to said first surface, said first surface being exposable to a plating solution, said substrate comprising

a conductive pattern being positioned at said first surface of a substrate;

a contact to the first surface of the substrate; and

said conductive pattern being temporary electrically connected by a polysilicon or an amorphous silicon conductor with said contact and said contact being electrically connected with said second surface.

In a further aspect of the invention, a method is disclosed for plating on at least one conductive pattern formed at a surface of a substrate, said substrate having at least a first surface and a second surface, said method comprising the steps of:

placing the substrate on an electrode being part of a plating holder such that said second surface of said substrate is in contact with said electrode and said conductive pattern is temporary electrically connected to said conductive pattern; and

applying a plating solution on said first surface of said substrate thereby inhibiting exposure of said second surface to said plating solution.

In another embodiment of the invention, a plating solution is disclosed wherein said electrode and said conductive pattern are temporary electrically connected by forming a polysilicon or an amorphous silicon conductor to temporary connect said conductive pattern with a contact to the substrate, said contact being formed on the first surface of the substrate, and by providing an electrical connection between said contact and said electrode. The resistance of the electrical connection between the contact and the electrode is substantially independent of the location of the contact on the first surface of the substrate. Therefore, to achieve a high degree of uniformity over the substrate of the plating process, preferably the length of the polysilicon or the amorphous silicon conductor should be kept as short as possible. On the other hand, one has to be able to easily cut the connection provided by the silicon or the amorphous

silicon conductor after the plating process. Therefore, preferably, the conductive pattern is positioned on a first die and said contact is positioned on a second die different from said first die. By doing so, the connection can by cut by dicing the substrate. More preferably, said first and said second die are adjacent dies.

In another embodiment of the invention a method is disclosed, wherein prior to applying the plating solution, a resist layer is deposited on said conductive pattern and patterned in order to create at least one covered area an at least one uncovered area, said uncovered area being exposable to said plating solution.

In an embodiment of the invention, as an example, a system and a method for selectively electroplating a plurality of aluminum patterns is disclosed. The aluminum patterns to be plated are formed on the front side of a silicon wafer with a p-type conductivity. Each aluminum pattern (Fig. 1) to be plated is connected by means of a polysilicon line to an aluminum contact to the p-type substrate region of the wafer at the front side of the wafer. This contact is positioned on an adjacent die. The polysilicon line is isolated from the wafer by means of at least one dielectric layer. The polysilicon line extends over a dicing line (Fig. 2). Accordingly, all aluminum patterns to be plated are electrically connected to the back side of the wafer which can be provided with an aluminum metal contact.

Before applying a plating solution, the wafer is placed on a support with an electrically connectable electrode thereon such that there is an electrical connection between the back side of the wafer and the electrode. This support is a part of a wafer holder designed for plating purposes. During the plating process, the plating solution is brought in contact with the front

side of the wafer, while the backside is sealed by means of a sealing element being part of the aforementioned wafer holder (Fig. 3). Particularly, this sealing element is a sealing ring which inhibits the exposure of the backside of the substrate to the plating solution The backside of the wafer is electrically connected with a backside electrode of the same size. By immersing a similar electrode as counter electrode in the plating solution, a homogeneous electrical field can be created. The plating process is galvanostatic, e.g. the current is held constant by regulating the potential between the backside and the counter electrode. According to the example, silver is electroplated and an alkaline silver solution is used as plating solution. A negative potential is applied at the backside electrode.

In order to avoid plating of the aluminium contacts to the substrate at the front side of the substrate, a positive photoresist layer (AZ4562) is used to cover those areas where no plating may occur.

Finally, the wafers are stripped and diced. Figure 4 and figure 5 show respectively a cross-section and top view of the polysilicon lines. By dicing over the polysilicon lines, the electroplated structures are disconnected from the respective substrate contact.

By using the substrate as a contacting layer for an electrode, the electrical resistance between the areas to be plated and the electrical contact point is for all plated structures substantially the same, particularly if the length of the polysilicon lines is kept sufficiently short and the specific resistance of the polysilicon line is sufficiently low. This length has to be sufficiently short to assure that the resistance of the polysilicon lines has a negligible contribution to the total resistance of the connection between the conductive pattern and the

backside of the wafer. Accordingly, the uniformity of the plating process is increased or in another words, the homogeneity of the deposited thickness of the plated material over the complete wafer is increased. In the example, the plated material is silver.

By dicing over the polysilicon lines, the individual electroplated patterns are disconnected one from the other and are no longer in contact with the substrate. By using polysilicon or amorphous silicon lines extending over the dicing lines, the risk to create electroplated patterns, being short-circuited to the substrate after dicing is reduced. If metal lines or leads would be used to provide the connection to the contact extending over the dicing line, the electroplated patterns can still be in contact with the substrate after dicing due to metal shavings or residues.

The same plating system and method as defined according the present invention can be used for electrochemical chloridation on wafer scale provided that a different solution is used and a positive potential is applied at the backside electrode instead of a negative potential. Of particular interest is the electrochemical chloridation of silver. The electrochemical chloridation of bulk silver electrodes (wires) can be used for producing standard reference electrodes. An advantage is that the quality of the AgCl layer formed by using electrochemical chloridation is better than by using a chemical chloridation. So, according to the present invention, Ag/AgCl reference electrodes on wafer scale can be formed by using electroplated silver and electrochemically chloridized silver chloride.

CLAIMS

1. A method for plating on at least one conductive pattern on a surface of a substrate, said substrate having at least a first surface and a second surface, said method comprising the steps of:

placing the substrate on an electrode being part of a plating holder such that said second surface of said substrate is in contact with said electrode and said conductive pattern is temporarily electrically connected to said electrode; and

applying a plating solution on said first surface of said substrate thereby inhibiting exposure of said second surface to said plating solution.

characterised in that said electrode and said conductive pattern are temporarily electrically connected by forming a polysilicon or an amorphous silicon conductor to temporarily connect said conductive pattern with a contact to the substrate, said contact being formed on the first surface of the substrate, and by providing an electrical connection between said contact and said electrode.

2. A method as recited in claim 1, wherein said conductive pattern is positioned on a first die and said contact is positioned on a second die different from said first die.

3. A method as recited in claim 2, wherein after said conductive pattern is plated, said method further comprises the step of dicing the substrate

4. A method as in claim 1, wherein prior to applying the plating solution, a resist layer is deposited on said conductive pattern and patterned in order to create at least one covered area an at least one uncovered area, said uncovered area being exposable to said plating solution.

5. A method as recited in claim 1, where said plating solution comprises an element selected from a group comprising Ag, Cu, Au, Pt, Ti, Ni and Co.

6. A substrate having at least a first surface and a second surface opposite to said first surface, said first surface being exposable to a plating solution, said substrate comprising

a conductive pattern being positioned at said first surface of a substrate;

a contact to the first surface of the substrate; and

said conductive pattern being temporarily electrically connected by a polysilicon or an amorphous silicon conductor with said contact and said contact being electrically connected with said second surface.

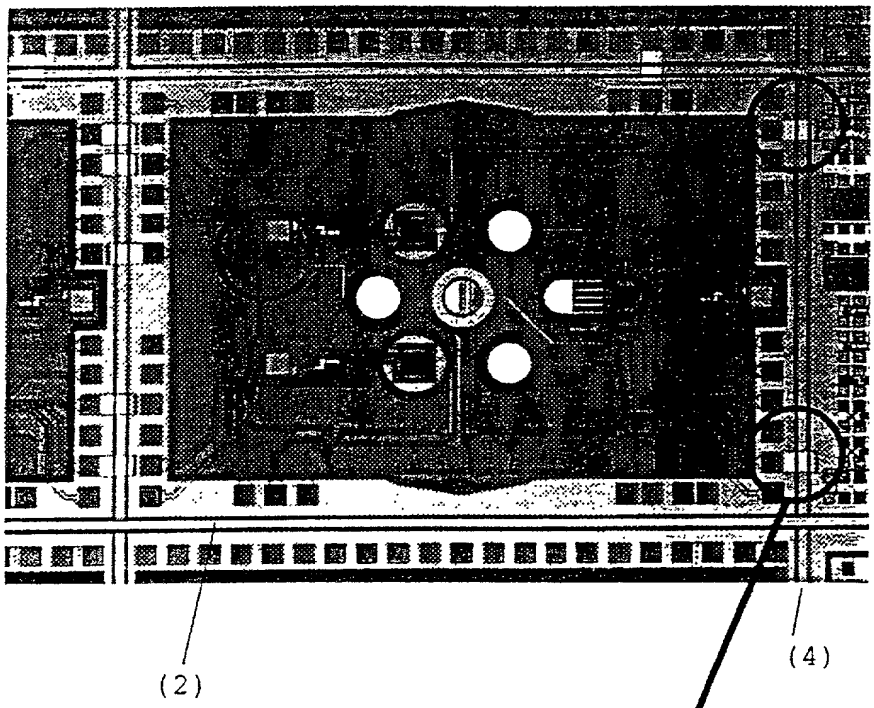
(2)
(4)

FIG. 1

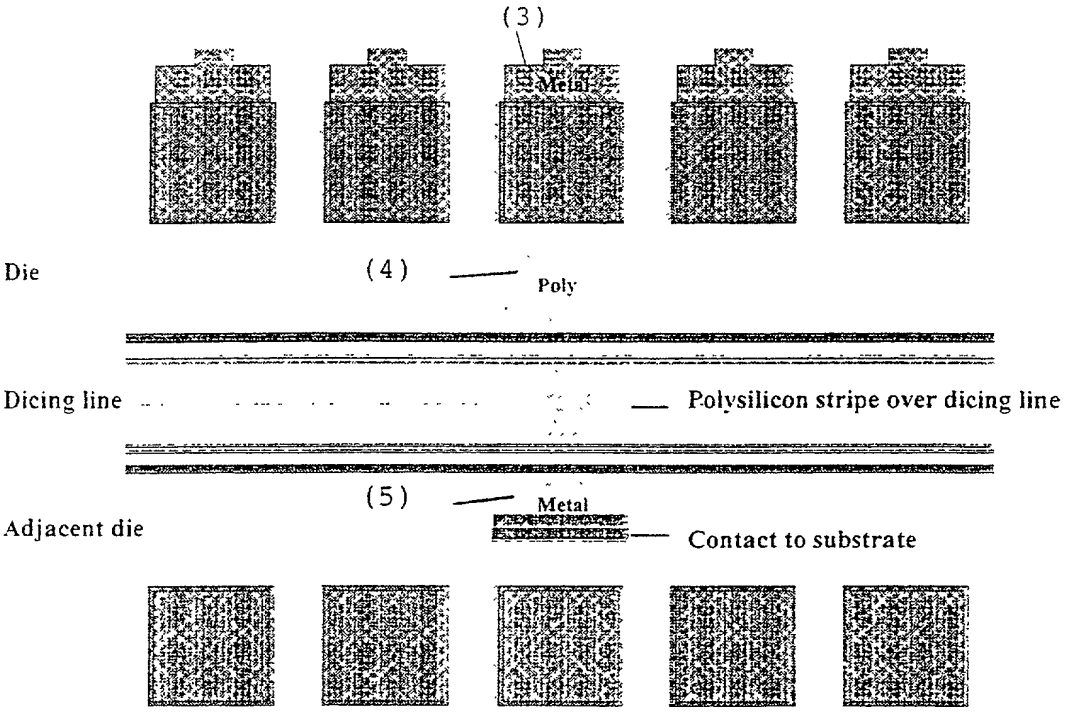
(3)
Metal
Die
(4)
Poly
Dicing line
Polysilicon stripe over dicing line
(5)
Metal
Adjacent die
Contact to substrate

FIG. 2

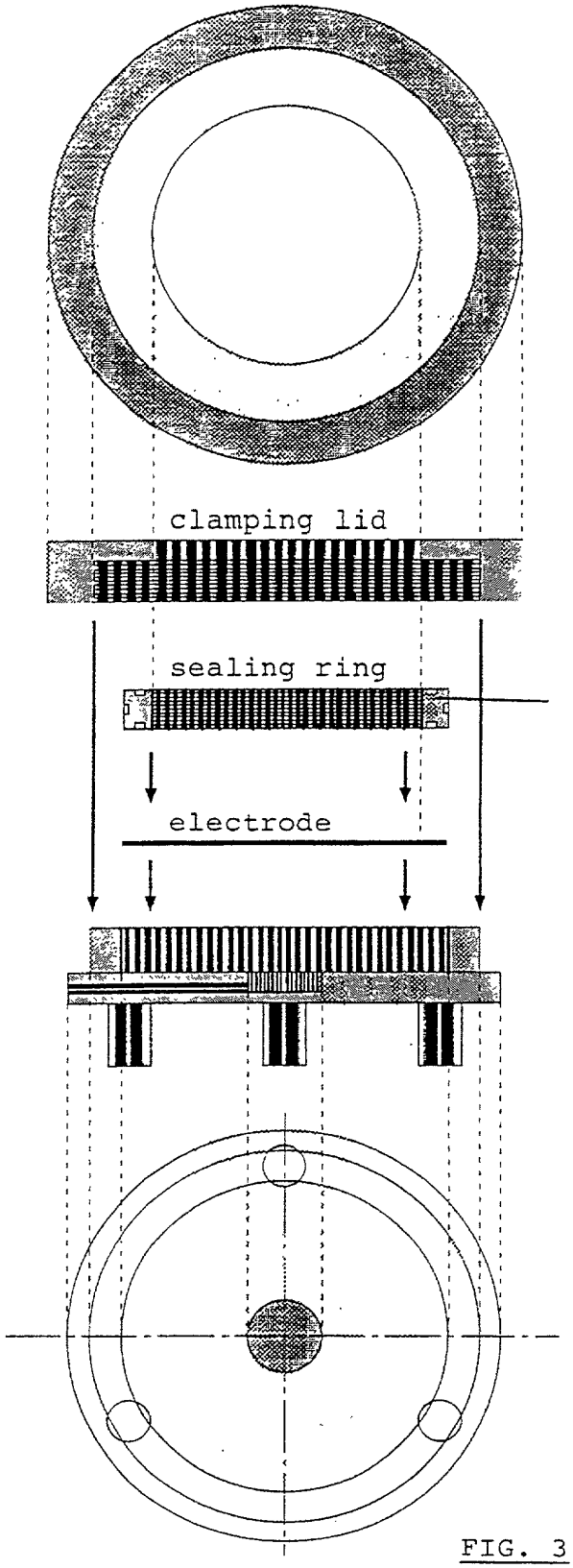

FIG. 3

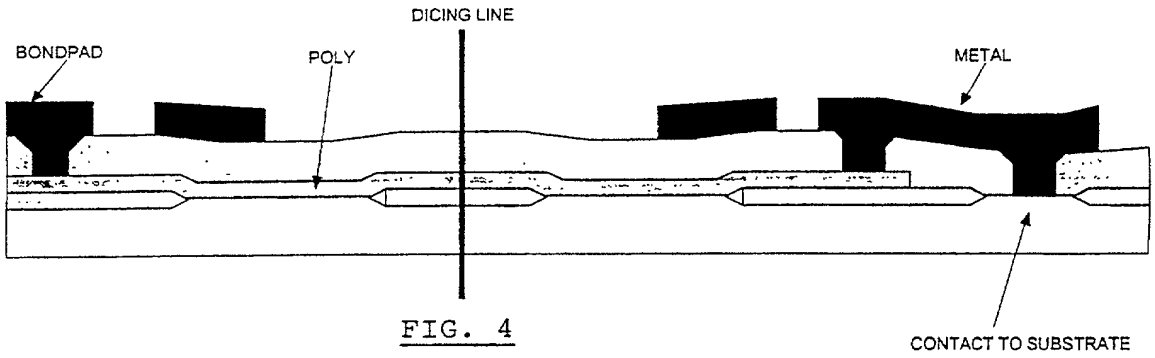

FIG. 4

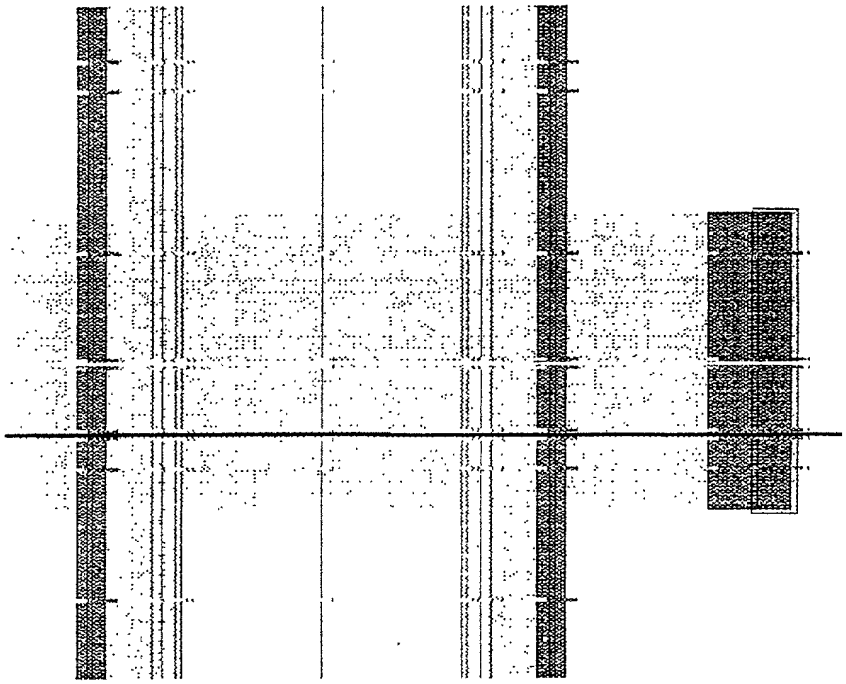

FIG. 5

DECLARATION - USA PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to our names;

I believe that I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled A SYSTEM AND A METHOD FOR PLATING OF A CONDUCTIVE PATERN; the specification of which was filed on **January 23, 2001** as Application Serial No. **09/744,465** and was amended on .

I hereby state that we have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above;

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56;

I hereby claim the benefit under Title 35, United States Codes § 119(e) of any United States provisional application(s) listed below.

Application No.: 06/093,974 Filing Date: July 24, 1998

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			Priority Claimed
No.: **PCT/BE99/00090**	Country: **Belgium**	Date Filed: **July 14, 1999**	**Yes**

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below, and insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code § 112, we acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first inventor: Filip Van Steenkiste

Inventor's signature ____________

Date 27/3/01

Residence: Hoevestraat 12, B-9870 Machelen, Belgium

Citizenship: ____________

Post Office Address: Hoevestraat 12, B-9870 Machelen, Belgium

Full name of second inventor: Kris Baert

Inventor's signature ____________

Date 14/3/01

Residence: St. Jorislaan 9, B-3001 Leuven, Belgium

Citizenship: ____________

Post Office Address: St. Jorislaan 9, B-3001 Leuven, Belgium

Full name of third inventor: Walter Gumbrecht

Inventor's signature ____________

Date ____________

Residence: In der Rote 1, D-91074 Herzogenaurach, Germany

Citizenship: ____________

Post Office Address: In der Rote 1, D-91074 Herzogenaurach, Germany

Full name of Fourth inventor: Philippe Arquint

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first inventor: Filip Van Steenkiste

Inventor's signature _____

Date _____

Residence: Hoevestraat 12, B-9870 Machelen, Belgium

Citizenship: _____

Post Office Address: Hoevestraat 12, B-9870 Machelen, Belgium

Full name of second inventor: Kris Baert

Inventor's signature _____

Date _____

Residence: St. Jorislaan 9, B-3001 Leuven, Belgium

Citizenship: _____

Post Office Address: St. Jorislaan 9, B-3001 Leuven, Belgium

Full name of third inventor: Walter Gumbrecht

Inventor's signature Walter Gumbrecht

Date 03/08/2001

Residence: In der Rote 1, D-91074 Herzogenaurach, Germany

Citizenship: German

Post Office Address: In der Rote 1, D-91074 Herzogenaurach, Germany

Full name of Fourth inventor: Philippe Arquint

4-ω

Inventor's signature Philipp Arquint

Date 03-19-2001

Residence: Stegerstrasse 13A, D-91074 Herzogenaurach, Germany DEX

Citizenship: Swiss

Post Office Address: Stegerstrasse 13A, D-91074 Herzogenaurach, Germany

Send Correspondence To:
KNOBBE, MARTENS, OLSON & BEAR, LLP
Customer No. 20,995

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IMEC228.001APC

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Van Steenkiste, et al.
App. No.	:	09/744,465
Filed	:	January 23, 2001
For	:	A SYSTEM AND A METHOD FOR PLATING OF A CONDUCTIVE PATTERN
Examiner	:	Unknown

ESTABLISHMENT OF RIGHT OF ASSIGNEE TO TAKE ACTION
AND
REVOCATION AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The undersigned is empowered to act on behalf of the assignees below (the "Assignees"). A true copy of the original Assignment of the above-captioned application from the inventors to the Assignees is attached hereto. This Assignment represents the entire chain of title of this invention from the Inventors to the Assignees.

We declare that all statements made herein are true, and that all statements made upon information and belief are believed to be true, and further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that willful, false statements may jeopardize the validity of the application, or any patent issuing thereon.

The undersigned hereby revokes any previous powers of attorney in the subject application, and hereby appoints the registrants of Knobbe, Martens, Olson & Bear, LLP, 620 Newport Center Drive, Sixteenth Floor, Newport Beach, California 92660, Telephone (949) 760-0404, **Customer No. 20,995**, as its attorneys with full power of substitution and

revocation to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected herewith. This appointment is to be to the exclusion of the inventors and their attorneys in accordance with the provisions of 37 C.F.R. § 3.71.

Please use **Customer No. 20,995** for all communications.

Interuniversitair Micro-Elektronica Centrum

Dated: _____ By: _____
Gilbert Declerck

Title: President

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